Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A split-gate non-volatile memory cell, comprising:
a substrate;
a charge-trapping layer on the substrate;
a split gate on the charge-trapping layer, including at least one split region directly over the charge-trapping layer; and
a source/drain in the substrate beside the split gate, wherein
the charge-trapping layer around the split region serves as a coding region.

[c2] 2. The split-gate non-volatile memory cell of claim 1, wherein the split gate consists of at least two pieces separated by a dielectric layer.

[c3] 3. The split-gate non-volatile memory cell of claim 2, wherein the split gate consists of three pieces.

[c4] 4. The split-gate non-volatile memory cell of claim 3, wherein the three pieces of the split gate include a pair of conductive spacers and a conductive layer between the pair of conductive spacers.

[c5] 5. The split-gate non-volatile memory cell of claim 4, wherein the pair of conductive spacers are arranged with two substantially vertical sidewalls thereof adjacent to the source/drain.

[c6] 6. The split-gate non-volatile memory cell of claim 5, further comprising an insulator on the source/drain, wherein the pair of conductive spacers are disposed on the sidewalls of the insulator.

[c7] 7. The split-gate non-volatile memory cell of claim 2, wherein different pieces of the split gate are electrically connected to each other.

[c8] 8. The split-gate non-volatile memory cell of claim 2, wherein the dielectric layer comprises silicon oxide.

[c9] 9. The split-gate non-volatile memory cell of claim 1, wherein the split gate comprises polysilicon.

[c10] 10. The split-gate non-volatile memory cell of claim 1, wherein the charge-trapping layer comprises a silicon nitride layer disposed between two silicon oxide layers.

[c11] 11. The split-gate non-volatile memory cell of claim 1, wherein the charge-trapping layer comprises aluminum oxide (Al_2O_3).

[c12] 12. The split-gate non-volatile memory cell of claim 1,

wherein the substrate comprises a p-substrate, and the source/drain comprises an n-type source/drain.

[c13] 13. A NAND non-volatile memory array, comprising:
a substrate;
an array of split-gate non-volatile memory cells on the substrate, each comprising a charge-trapping layer and a split gate thereon and sharing a diffusion with an adjacent memory cell in the same row, wherein the split gate includes at least one split region directly over the charge-trapping layer, and the charge-trapping layer around the split region serves as a coding region;
a plurality of word lines, each coupled to the split gates of the memory cells in one column; and
a plurality of bit lines and a plurality of source regions, wherein a pair of bit line and source region are coupled to one terminal memory cell and the other terminal memory cell, respectively, in a row of memory cells.

[c14] 14. The NAND non-volatile memory array of claim 13, wherein each split gate consists of at least two pieces separated by a dielectric layer.

[c15] 15. The NAND non-volatile memory array of claim 14, wherein the dielectric layer comprises silicon oxide.

[c16] 16. The NAND non-volatile memory array of claim 14,

wherein a split gate of a memory cell is directly a portion of the word line coupled to the memory cell.

[c17] 17. The NAND non-volatile memory array of claim 16, wherein a word line comprises:
a boundary conductor at a boundary of the memory array; and
a split gate line, comprising a pair of linear conductive spacers crossing the memory array and directly connected with the boundary conductor, and a linear conductor between the pair of linear conductive spacers and separated from the boundary conductor and the pair of linear conductive spacers by the dielectric layer, wherein the linear conductor and the boundary conductor together are connected with a contact.

[c18] 18. The NAND non-volatile memory array of claim 17, wherein the pair of linear conductive spacers are arranged with two substantially vertical sidewalls thereof adjacent to the diffusions.

[c19] 19. The NAND non-volatile memory array of claim 13, wherein one terminal memory cell in a row of memory cells is coupled to a bit line via a first select transistor.

[c20] 20. The NAND non-volatile memory array of claim 19, wherein the other terminal memory cell in the row of

memory cells is coupled to a source via a second select transistor.

[c21] 21. The NAND non-volatile memory array of claim 13, wherein two adjacent rows of memory cells share a source region.

[c22] 22. The NAND non-volatile memory array of claim 21, wherein 2×8 (row× column) memory cells are partitioned as a unit that is coupled to two bit lines and one source region.

[c23] 23. The NAND non-volatile memory array of claim 13, wherein the memory cells are disposed on a p-well in the substrate, and the substrate is an n-substrate.

[c24] 24. The NAND non-volatile memory array of claim 13, wherein the split gates comprise polysilicon.

[c25] 25. The NAND-type non-volatile memory array of claim 13, wherein the charge-trapping layer comprises a silicon nitride layer disposed between two silicon oxide layers.

[c26] 26. The NAND-type non-volatile memory array of claim 13, wherein the charge-trapping layer comprises aluminum oxide (Al_2O_3).

[c27] 27. A split-gate non-volatile memory array, comprising:

a substrate;

an array of split-gate non-volatile memory cells on the substrate, each comprising a charge-trapping layer, a split gate on the charge-trapping layer and two diffusions in the substrate beside the split gate, wherein the split gate includes at least one split region directly over the charge-trapping layer, and the charge-trapping layer around the split region serves as a coding region;

a plurality of word lines, each coupled to the split gates of the memory cells in one column; and

a plurality of bit lines, each coupled to the memory cells in one row via the diffusions.

[c28] 28. The split-gate non-volatile memory array of claim 27, wherein the split-gate non-volatile memory cells are arranged in a NAND-type, NOR-type or AND-type configuration.

[c29] 29. The split-gate non-volatile memory array of claim 27, wherein each split gate consists of at least two pieces separated by a dielectric layer.

[c30] 30. The split-gate non-volatile memory array of claim 29, wherein the dielectric layer comprises silicon oxide.

[c31] 31. The split-gate non-volatile memory array of claim 29, wherein a split gate of a memory cell is directly a

portion of the word line coupled to the memory cell.

[c32] 32. The split-gate non-volatile memory array of claim 31, wherein a word line comprises:

a boundary conductor at a boundary of the non-volatile memory array; and

a split gate line on the charge-trapping layer crossing the non-volatile memory array, comprising at least a first linear conductor and a second linear conductor completely or partially covered by the first linear conductor, wherein

the second linear conductor is directly connected with the boundary conductor;

the first linear conductor is separated from the second linear conductor and the boundary conductor by a dielectric layer; and

the first linear conductor and the boundary conductor together are connected with a contact.

[c33] 33. The split-gate non-volatile memory array of claim 32, wherein

the split gate line further comprises a third linear conductor;

the second and the third linear conductors are formed as a pair of linear spacers each having a non-vertical sidewall and a substantially vertical sidewall; and

the first linear conductor is between the second and the

third linear conductors; wherein each of the second and the third linear conductors is arranged so that the non-vertical sidewall thereof faces the first linear conductor.

[c34] 34. The split-gate non-volatile memory array of claim 33, wherein a top portion of the first linear conductor completely covers the second and the third linear conductors.

[c35] 35. An operating method of a split-gate non-volatile memory cell, wherein
the split-gate non-volatile memory cell comprises:
a substrate;
a charge-trapping layer on the substrate;
a split gate on the charge-trapping layer, including at least one split region directly over the charge-trapping layer, wherein the charge-trapping layer around the split region serves as a coding region; and
a source/drain in the substrate beside the split gate, and
the operating method comprises:
in a programming operation:
applying 0V to the substrate and the source/drain; and
applying a first negative voltage to the split gate, the first negative voltage being sufficiently high for injecting electrons into the coding region; and
in an erasing operation:
applying 0V to the split gate;

floating the source/drain; and
applying a second negative voltage to the substrate, the second positive voltage being sufficiently high for ejecting electrons from the coding region.

[c36] 36. The operating method of claim 35, wherein the first negative voltage is about 10V.

[c37] 37. The operating method of claim 35, wherein the second negative voltage is about 10V.

[c38] 38. An operating method of a NAND non-volatile memory array, wherein
the NAND non-volatile memory array comprises:
a substrate;
an array of split-gate non-volatile memory cells on the substrate, each comprising a charge-trapping layer and a split gate thereon and sharing a diffusion with an adjacent memory cell in the same row, wherein the split gate includes at least one split region directly over the charge-trapping layer, and the charge-trapping layer around the split region serves as a coding region;
a plurality of word lines, each coupled to the split gates of the memory cells in one column; and
a plurality of bit lines and a plurality of source regions, wherein a pair of bit line and source region are coupled to one terminal memory cell and the other terminal

memory cell, respectively, in a row of memory cells; and the operating method comprises:

in a programming operation:

applying 0V to the substrate and a selected bit line and a source coupled to a selected memory cell;

applying a first negative voltage to a selected word line coupled to a selected memory cell, the first negative voltage being sufficiently high for injecting electrons into the charge-trapping layer of the selected memory cell;

applying a first positive voltage to unselected word lines to turn on unselected memory cells in the same row; and

applying a second negative voltage to unselected bit lines to inhibit programming of the unselected memory cells that are coupled to the selected word line together with the selected memory cell, and

in an erasing operation,

applying 0V to the word lines;

applying a third negative voltage to the substrate, the third negative voltage being sufficiently high for ejecting electrons from the charge-trapping layers of the memory cells; and

floating the bit lines and the source regions.

[c39] 39. The operating method of claim 38, wherein the first negative voltage is about 10V.

[c40] 40. The operating method of claim 38, wherein the first positive voltage is about 3V.

[c41] 41. The operating method of claim 38, wherein the second negative voltage is about 4V.

[c42] 42. The operating method of claim 38, wherein the third negative voltage is about 10V.

[c43] 43. The operating method of claim 38, wherein one terminal memory cell in a row of memory cells is coupled to a bit line via a first select transistor and the other terminal memory cell in the same row of memory cells is coupled to a source via a second select transistor, and the operating method further comprises:
in the programming operation, applying a second positive voltage to a gate of the first select transistor to turn on the first select transistor, and applying 0V to a gate of the second select transistor; and
in the erasing operation, applying a fourth negative voltage to the gates of the first and the second select transistors.

[c44] 44. The operating method of claim 43, wherein the second positive voltage is about 10V.

[c45] 45. The operating method of claim 43, wherein the fourth negative voltage is about 10V.